

**EUROPEAN PATENT APPLICATION**

(51) Int Cl.<sup>6</sup>: **H04N 3/15**

(22) Date of filing: 31.07.1996

(72) Inventor: **Takahashi, Hidekazu**  
**Tokyo (JP)**

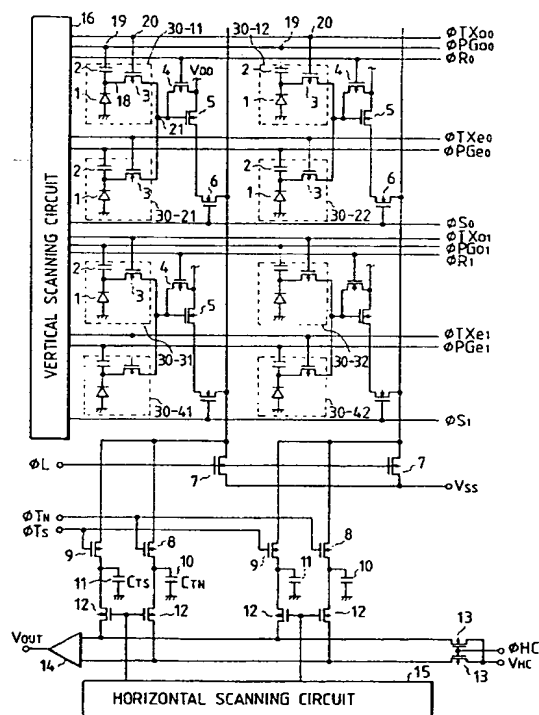
(74) Representative:  
**Beresford, Keith Denis Lewis et al**  
**BERESFORD & Co.**  
**2-5 Warwick Court**  
**High Holborn**  
**London WC1R 5DJ (GB)**

(71) Applicant: **CANON KABUSHIKI KAISHA**  
**Tokyo (JP)**

(54) Solid state image pickup apparatus

(57) In order to realize a multi-function sensor in which in a pixel portion an addition and a non-addition can be arbitrarily performed, there is provided a solid state image pickup apparatus in which charges generated by a photoelectric converting device are transferred to a floating diffusion portion through a transfer switch and a change in electric potential of the floating diffusion portion is outputted by a source-follower. Some photoelectric converting devices are connected to one floating diffusion portion through the transfer switch. One set of source-follower are formed for a few pixels. The photoelectric converting device is constructed by an MOS transistor gate and a depletion layer under the gate.

FIG. 1



## Description

### BACKGROUND OF THE INVENTION

#### Field of the Invention

The invention relates to an image pickup apparatus for obtaining an image signal and, more particularly, to a solid state image pickup apparatus of an amplifying type of a CMOS process compatible XY address type.

#### Related Background Art

Hitherto, a solid state image pickup device has an MOS structure comprising a metal which can perform a photoelectric conversion, an oxide, and a semiconductor and is mainly classified into an FET type and a CCD type in accordance with a moving system of a light carrier. The solid state image pickup device is used in various fields such as solar cell, imaging camera, copying machine, facsimile, and the like and techniques such as converting efficiency and an integration density have been improved. As one of such amplifying type solid state image pickup apparatuses, there is a sensor of a CMOS process compatible type (hereinafter, abbreviated as a CMOS sensor). Such a type of sensor has been published in a literature such as "IEEE Transactions on Electron Device", Vol. 41, pp 452-453, 1994, or the like. Fig. 11B shows a circuit constructional diagram of a CMOS sensor. Fig. 11A shows a cross sectional view thereof. Fig. 11C shows a state diagram of charges during the accumulation of photons  $h\nu$  of a photoelectric converting unit. Fig. 11D shows a state diagram of charges after the photons  $h\nu$  were accumulated.

In Figs. 11A and 11B, reference numeral 1 denotes a photoelectric converting unit; 2 a photo gate by an MOS transistor; 3 a transfer switch MOS transistor; 4 an MOS transistor for resetting; 5 a source-follower amplifier MOS transistor; 6 a horizontal selection switch MOS transistor; 7 a source-follower load MOS transistor; 8 a dark output transfer MOS transistor; 9 a light output transfer MOS transistor; 10 a dark output accumulating capacitor; 11 a light output accumulating capacitor.

Reference numeral 17 denotes a p-type well; 18 a gate oxide film; 19 first layer polysilicon; 20 second layer polysilicon; and 21 an  $n^+$  floating diffusion region (FD). One of the features of the present sensor is that the sensor is full CMOS transistor process compatible and an MOS transistor of a pixel portion and an MOS transistor of a peripheral circuit can be formed by the same processing step, so that the number of masks and the number of processing steps can be remarkably reduced as compared with those of a CCD.

An operating method will now be simply explained. First, a positive voltage is applied to a control pulse  $\phi_{PG}$  in order to extend a depletion layer under the photo gate 2. The FD portion 21 sets a control pulse  $\phi_R$  to the H level and is fixed to a power source  $V_{DD}$  in order to pre-

vent a blooming during the accumulation. When the photons  $h\nu$  are irradiated and carriers occur under the photo gate 2, electrons are accumulated in the depletion layer under the photo gate 2 and holes are ejected through the p-type well 17.

Since an energy barrier by the transfer MOS transistor 3 is formed among the photoelectric converting unit 1, p-type well 17, and FD portion 21, the electrons exist under the photo gate 2 during the accumulation of the photo charges (Fig. 11C). When the apparatus enters a reading mode, the control pulse  $\phi_{PG}$  and a control pulse  $\phi_{TX}$  are set so as to eliminate the barrier under the transfer MOS transistor 3 and to completely transfer the electrons under the photo gate 2 to the FD portion 21 (Fig. 11D). Since the complete transfer is executed, an after-image and noises are not generated in the photoelectric converting unit 1. When the electrons are transferred to the FD portion 21, an electric potential of the FD portion 21 changes in accordance with the number of electrons. By outputting a potential change to the external horizontal selection switch MOS transistor 6 through a source of the source-follower amplifier MOS transistor 5 by the source-follower operation, photoelectric converting characteristics of a good linearity can be obtained. Although kTC noises by resetting are generated in the FD portion 21, they can be eliminated by sampling and accumulating a dark output before the transfer of light carriers and obtaining a difference between the dark output and the light output. The CMOS sensor is, therefore, characterized by low noises and a high S/N signal. Since the complete non-destructive reading is performed, multi-functions can be realized. Further, there are also advantages such that a high yield due to an XY address system and a low electric power consumption are obtained.

The above conventional apparatus, however, has drawbacks such that since one photo gate, four MOS transistors, and four horizontal driving lines exist for each pixel, as compared with the sensor of the CCD type, it is difficult to reduce the number of pixels and a numerical aperture also decreases.

There is also a drawback such that since the addition of the photoelectric conversion signals to perform a TV scan is also executed by a peripheral circuit, an operating speed becomes slow.

### SUMMARY OF THE INVENTION

Embodiments of the invention realize a reduction of a CMOS sensor.

Embodiments of the invention realize an execution of an addition of pixel signals by a pixel unit and, further, realize a multi-function sensor which can arbitrarily execute an addition and a non-addition.

The present invention is characterized in that an FD region and a source-follower amplifier provided hitherto for every pixel are formed for a few pixels and a plurality of photoelectric converting regions are connected to the

FD region through an MOS transistor switch.

With such a construction, since it is sufficient that one set of a source-follower MOS transistor amplifier, an MOS transistor for selecting a horizontal line, and an MOS transistor for resetting are provided at a few pixel periods of time, the number of devices and the number of wirings which are occupied in each pixel can be reduced than the conventional ones, so that a fine structure can be accomplished.

Since the addition and the non-addition of the signal charges of two pixels can be easily performed at a timing of the transfer MOS transistor to the FD unit, the invention can cope with various driving methods such as color difference line sequential driving, whole pixel independent output driving, and the like.

In the solid state image pickup apparatus, further, the invention is characterized in that the photoelectric converting device comprises an MOS transistor gate and a depletion layer under the gate. It is also characterized in that the MOS transistor gate of the photoelectric converting device is formed by the same processing steps as those of the MOS transistor of the peripheral circuit. It is also characterized in that the photoelectric converting device is a pn junction photodiode. It is further characterized in that the charges of the plurality of photoelectric converting devices can be simultaneously or separately transferred to the floating diffusion portion. It is also characterized by an image pickup apparatus for obtaining image signal outputs by arranging a plurality of solid state image pickup apparatuses. With such a construction, a variety of image signals can be obtained.

The above and other objects and features of the present invention will become apparent from the following detailed description and the appended claims with reference to the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic circuit constructional diagram of the first embodiment according to the invention;  
 Fig. 2 is a cross sectional view of a pixel in the first embodiment according to the invention;  
 Fig. 3 is a timing chart (1) in the first embodiment according to the invention;  
 Fig. 4 is a timing chart (2) in the first embodiment according to the invention;  
 Fig. 5 is a schematic circuit constructional diagram of the second embodiment according to the invention;  
 Fig. 6 is a diagram of an on-chip color filter in the second embodiment according to the invention;  
 Fig. 7 is a schematic circuit constructional diagram of the third embodiment according to the invention;  
 Fig. 8 is a schematic circuit constructional diagram of the fourth embodiment according to the invention;  
 Fig. 9 is a cross sectional view of a pixel in the fourth

embodiment according to the invention;

Fig. 10 is a cross sectional view of a pixel in the fifth embodiment according to the invention; and  
 Figs. 11A to 11D are schematic circuit constructional diagrams of a conventional solid state image pickup apparatus.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will now be described in detail hereinbelow with reference to the drawings.

Fig. 1 shows a schematic circuit constructional diagram of the first embodiment according to the invention. In the diagram, although a 2-dimensional area sensor of (2 columns  $\times$  4 rows) pixels is shown, actually, the sensor is magnified and the number of pixels is increased to (1920 columns  $\times$  1080 rows) or the like, thereby raising a resolution.

In Fig. 1, reference numeral 1 denotes the photoelectric converting unit of a photoelectric converting device comprising an MOS transistor gate and a depletion layer under the gate; 2 the photo gate; 3 the transfer switch MOS transistor; 4 the MOS transistor for resetting; 5 the source-follower amplifier MOS transistor; 6 the horizontal selection switch MOS transistor; 7 the source-follower load MOS transistor; 8 the dark output transfer MOS transistor; 9 the light output transfer MOS transistor; 10 the dark output accumulating capacitor  $C_{TN}$ ; 11 the light output accumulating capacitor  $C_{TS}$ ; 12 a horizontal transfer MOS transistor; 13 a horizontal output line resetting MOS transistor; 14 a differential output amplifier; 15 a horizontal scanning circuit; and 16 a vertical scanning circuit.

Fig. 2 shows a cross sectional view of a pixel portion. In the diagram, reference numeral 17 denotes the p-type well; 18 the gate oxide film; 19 the first layer polysilicon; 20 the second layer polysilicon; and 21 the n<sup>+</sup> floating diffusion (FD) portion. The FD portion 21 is connected to another photoelectric converting unit through another transfer MOS transistor. In the diagram, drains of two transfer MOS transistors 3 and the FD portion 21 are commonly constructed, thereby realizing a fine structure and the improvement of a sensitivity due to a reduction of a capacitance of the FD portion 21. The FD portion 21, however, can be also connected by an Al wiring.

The operation will now be described with reference to a timing chart of Fig. 3. The timing chart relates to a case of a whole pixel independent output.

First, a control pulse  $\phi_L$  is set to the high (H) level by a timing output from the vertical scanning circuit 16 and a vertical output line is reset. Control pulses  $\phi_{R0}$ ,  $\phi_{PGq0}$ , and  $\phi_{PGe0}$  are set to the high level, the MOS transistor 4 for resetting is turned on, and the first layer polysilicon 19 of the photo gate 2 is set to the H level. At time  $T_0$ , a control pulse  $\phi_{S0}$  is set to the H level, the

selection switch MOS transistor 6 is turned on, and the pixel portions of the first and second lines are selected. The control pulse  $\phi R0$  is subsequently set to the low (L) level, the resetting of the FD portion 21 is stopped, the FD portion 21 is set to the floating state, and a circuit between the gate and source of the source-follower amplifier MOS transistor 5 is set into a through state. After that, at time T1, a control pulse  $\phi TN$  is set to the H level, thereby allowing a dark voltage of the FD portion 21 to be outputted to the accumulating capacitor  $C_{TN}$  10 by the source-follower operation.

Subsequently, in order to perform a photoelectric conversion output of the pixels of the first line, a control pulse  $\phi TXo0$  of the first line is set to the H level and the transfer switch MOS transistor 3 is made conductive. After that, at time T2, the control pulse  $\phi PGo0$  is set to the L level. In this instance, it is preferable to set to a voltage relation such as to raise a potential well extending under the photo gate 2 and to allow the light generation carriers to be perfectly transferred to the FD portion 21. Therefore, so long as the complete transfer can be performed, the control pulse  $\phi TX$  is not limited to a pulse but can be also set to a fixed electric potential.

At time T2, since the charges from the photoelectric converting unit 1 of the photodiode are transferred to the FD portion 21, the electric potential of the FD portion 21 changes in accordance with the light. In this instance, since the source-follower amplifier MOS transistor 5 is in a floating state, a control pulse  $\phi Ts$  is set to the H level at time T3 and the electric potential of the FD portion 21 is outputted to the accumulating capacitor  $C_{TS}$  11. At this time point, the dark output and light output of the pixels of the first line have been accumulated in the accumulating capacitors  $C_{TN}$  10 and  $C_{TS}$  11, respectively. A control pulse  $\phi HC$  at time T4 is temporarily set to the H level, the horizontal output line resetting MOS transistor 13 is made conductive, and the horizontal output line is reset. The dark output and light output of the pixels are outputted to the horizontal output line in a horizontal transfer period of time by a scanning timing signal of the horizontal scanning circuit 15. At this time, when a differential output  $V_{OUT}$  is obtained by the differential output amplifier 14 of the accumulating capacitors  $C_{TN}$  10 and  $C_{TS}$  11, a signal of a good S/N ratio from which random noises and fixed pattern noises of the pixels have been eliminated is obtained. Although photo charges of pixels 30-12 and 30-22 are respectively accumulated in the accumulating capacitors  $C_{TN}$  10 and  $C_{TS}$  11 simultaneously with pixels 30-11 and 30-21, upon reading, a timing pulse from the horizontal scanning circuit 15 is delayed by a time corresponding to one pixel and the charges are read out to the horizontal output line and are generated from the differential output amplifier 14.

In the embodiment, although a construction such that the differential output  $V_{OUT}$  is executed in the chip has been shown, a similar effect can be also obtained even if a conventional CDS (Correlated Double Sampling) circuit is used in the outside without including such

a construction into the chip.

After the light output was outputted to the accumulating capacitor  $C_{TS}$  11, the control pulse  $\phi R0$  is set to the H level, the MOS transistor 4 for resetting is made conductive, and the FD portion 21 is reset to the power source  $V_{DD}$ . After completion of the horizontal transfer of the first line, the second line is read out. Upon reading out the second line, control pulses  $\phi TXe0$  and  $\phi PGe0$  are similarly driven, high level pulses are supplied as control pulses  $\phi TN$  and  $\phi TS$ , photo charges are accumulated into the accumulating capacitors  $C_{TN}$  10 and  $C_{TS}$  11, and the dark output and light output are taken out, respectively. By the above driving, the reading operations of the first and second lines can be independently executed. After that, a vertical scanning circuit is made operative and the reading operations of the  $(2n+1)$ th,  $(2n+2)$ th, ... lines ( $n = 1, 2, \dots$ ) are similarly executed, so that the outputs of all of the pixels can be independently performed. Namely, in case of  $n = 1$ , first, a control pulse  $\phi S1$  is set to the H level and a control pulse  $\phi R1$  is subsequently set to the L level. After that, control pulses  $\phi TN$  and  $\phi TXo1$  are set to the H level, a control pulse  $\phi PGo1$  is set to the L level, a control pulse  $\phi TS$  is set to the H level, and the control pulse  $\phi HC$  is temporarily set to the H level, thereby reading out pixel signals of pixels 30-31 and 30-32, respectively. Subsequently, control pulses  $\phi TXe1$  and  $\phi PGe1$  are supplied and the control pulses are applied in a manner similar to those mentioned above, thereby reading out pixel signals of pixels 30-41 and 30-42, respectively.

In the embodiment, since one set of source followers are not provided for one pixel but one set of source followers are provided for two pixels, the numbers of source-follower amplifier MOS transistors 5, selection switch MOS transistors 6, and resetting MOS transistors 4 can be reduced into 1/2 of the conventional ones. Thus, the numerical aperture of the photoelectric converting unit of the pixel is improved. A fine structure due to an integration of the pixel can be realized. By commonly using the FD portion 21 for two pixels, there is no need to increase a capacitance of the gate portion of the source-follower amplifier MOS transistor 5, so that a deterioration in sensitivity can be prevented.

As another feature of the invention, a point such that the S/N ratio can be improved by adding the signals of two or more pixels in the FD portion 21 can be also mentioned. Such a construction can be realized by changing only a timing of an applying pulse without substantially changing the circuit construction. Fig. 4 shows a timing chart in case of the addition of the pixel signals of two upper and lower pixels. In Fig. 3 showing the non-adding mode, the timings of the control pulses  $\phi TXo0$  and  $\phi TXe0$  and the timings of the control pulses  $\phi PGo0$  and  $\phi PGe0$  have been respectively shifted by a time of one pixel. However, they are the same timing in case of the addition. That is, since the pixel signals are simultaneously read out from the pixels 30-11 and 30-21, and the control pulse  $\phi TN$  is first set to the H level, a noise com-

ponent is read out from the vertical output line. The control pulses  $\phi TX_{00}$  and  $\phi TX_{e0}$  and the control pulses  $\phi PGe0$  and  $\phi PGe1$  are respectively simultaneously set to the H and L levels and are transferred to the FD portion 21. Thus, the signals of the two upper and lower photoelectric converting units 1 can be added by the FD portion 21 at the same time. Therefore, if two timings by the timing chart in Fig. 3 are prepared, for example, a mode for performing a high resolution image pickup in a bright state and, for example, in a dark state, a mode to execute a high sensitivity image pickup at a simultaneous reading timing by the timing chart of Fig. 4 can be realized by one sensor.

Although the above embodiment has been shown with respect to the example in which two photoelectric converting units are connected to the FD portion 21, a plurality of (for example, 3, 4, or the like) photoelectric converting units can be also connected. With such a structure, for example, an apparatus which can be applied to a wide field such as solid state image pickup apparatus of a high sensitivity, an apparatus of a high density, and the like can be provided by short processing steps by the CMOS process.

In the embodiment, each of the MOS transistors of a pixel portion 30 have been constructed by n type and the manufacturing steps have been simplified. However, it is also obviously possible to construct by all of the PMOS transistors by using an n-type well for a p-type substrate or vice versa.

Fig. 5 shows a schematic circuit diagram of the second embodiment according to the invention. The embodiment is characterized by providing a transfer switch 22 so that a color difference line sequential driving can be performed. In the first embodiment, although the addition of the first and second lines and the addition of the third and fourth lines can be performed, the addition of the second and third lines cannot be performed. In the embodiment, since the transfer switch 22 exists, the addition of the second and third lines can be executed.

In case of adding the second and third lines, when the first line is read out, the operation advances from time T0 to time T4 at a timing in Fig. 3 and, after that, when reading out the second line, the control pulses  $\phi TX_{e0}$  and  $\phi TX_{o1}$  and the control pulses  $\phi PGe0$  and  $\phi PGe1$  are simultaneously set to the H level and the low level, the control pulse  $\phi F$  is also set to the high level simultaneously with the control pulse  $\phi TX_{e0}$ , and the other control pulses are also similarly supplied. The pixel signals of the pixels 30-21 and 30-31 are accumulated in the accumulating capacitor 11. The noise components can be cancelled and the pixel signal output  $V_{OUT}$  can be obtained. After that, the pixel signals of pixels 30-22 and 30-32 are accumulated into the accumulating capacitor 11 and a pixel signal output  $V_{OUT}$  can be obtained. Subsequently, by supplying similar control pulses with respect to the third and fourth lines and pixel signals of pixels 30-31 and 30-41 and pixel signals of pixels 30-32 and 30-42 can be sequentially read out.

Therefore, if a complementary color mosaic type filter as shown in Fig. 6 is formed on the circuit construction chip of Fig. 5, according to the scan of the NTSC system, outputs of  $(C_y + M_g)$  and  $(Y_e + G)$  as sums of, for example, the first and second lines and outputs of  $(C_y + G)$  and  $(Y_e + M_g)$  as sums of, for example, the third and fourth lines can be sequentially obtained in an ODD (odd number) field. Even in an EVEN (even number) field, outputs of  $(C_y + M_g)$  and  $(Y_e + G)$  as sums of, for example, the second and third lines and outputs of  $(C_y + G)$  and  $(Y_e + M_g)$  as sums of, for example, the third and fourth lines can be sequentially obtained. Two carrier chrominance signals of the I axis (orange and cyan system) and the Q axis (green and magenta system) in the TV scan (NTSC, HD) of the interlace scan can be easily formed.

In the embodiment as well, it will be also obviously understood that outputs of all of the pixels can be independently performed by changing a supplying timing of the drive timing. Namely, if a control pulse  $\phi F$  is always set to the L level, the operation of the transfer switch 22 is turned off and the pixel signals can be read out every output of each pixel in accordance with a time sequence on the basis of the timing shown in Fig. 3.

According to the embodiment, therefore, the sum signal of the pixels which are deviated by one line can be outputted. Not only the apparatus can cope with the TV scan but also the pixel signals can be time sequentially independently read out every pixel or the sum signals of two pixels can be read out. Therefore, a variety of image pickup operations can be performed in accordance with the image pickup environment.

In the embodiment, in particular, if the color difference line sequential driving (interlace, color signal addition output) system is performed, the memory and the external adding circuit which are necessary for the first embodiment become unnecessary and the conventional signal processing circuit for a CCD can be used as it is. Therefore, it is advantageous in terms of costs and an installation.

Fig. 7 shows a conceptual circuit diagram of the third embodiment according to the invention. The embodiment is characterized in that, when the pixel signals are added, a switch MOS transistor 23 which can perform not only the addition in the FD portion by the timing shown in Fig. 4 but also the addition in the photoelectric converting unit is provided.

In Fig. 7, a timing of each control pulse is similar to that in the second embodiment. After the first line was read out, even when the second and third lines are subsequently read out, the control pulse  $\phi F$  is also set to the H level simultaneously with the control pulse  $\phi TX_{e0}$ . The charges of the photoelectric converting unit 1 of the pixel 30-21 and the charges of the photoelectric converting unit 1 of the pixel 30-31 are added by making the switch MOS transistor 23 conductive. The added charges are transferred to the accumulating capacitor 11 through the source-follower MOS transistor 5 and se-

lection switch MOS transistor 6 by making the transfer MOS transistor 3 of the pixel 30-21 conductive.

By forming the complementary color mosaic type filter shown in Fig. 6, in a manner similar to the second embodiment, outputs of  $(C_y + M_g)$  and  $(Y_e + G)$  as sums of, for example, the first and second lines and outputs of  $(C_y + G)$  and  $(Y_e + M_g)$  as sums of, for example, the third and fourth lines can be sequentially obtained in the ODD (odd number) field. Outputs of  $(C_y + M_g)$  and  $(Y_e + G)$  as sums of, for example, the second and third lines and outputs of  $(C_y + G)$  and  $(Y_e + M_g)$  as sums of, for example, the third and fourth lines can be sequentially obtained in the EVEN (even number) field.

Therefore, in the interlace driving, the addition is performed in the FD portion in the ODD field and the other charges are transferred to the other well and are added by the pixel portion in the EVEN field and the added charges are outputted to the FD portion. The above operations can be also obviously reversed in the EVEN field and the ODD field. In the embodiment, the TV scan can be performed without increasing the capacitance of the FD portion. By variably changing the timing of each control pulse, a variety of image signals can be also obtained in a manner similar to the second embodiment. Further, even in the embodiment, by executing a color difference line sequential driving in a manner similar to the second embodiment, there is an advantage such that the conventional signal processing circuit can be used as it is.

Fig. 8 shows a conceptual circuit diagram of the fourth embodiment according to the invention. The embodiment is characterized in that no photo gate is used in the photoelectric converting unit but a pn photodiode 24 is used. Fig. 9 shows a cross sectional view of a pixel. In the diagram, reference numeral 25 denotes an n-type layer having a density such that it can be perfectly formed to a depletion layer. Charges generated by the control pulse  $\phi_{TX}$  are completely transferred to the FD portion. In this case of the embodiment as well, the addition and non-addition of signals can be executed by control pulses  $\phi_{TX}$  even in the fourth embodiment.

The operation of Figs. 8 and 9 will be described. First, the control pulse  $\phi_R$  is set to the H level and the FD portion 21 is reset to the power source voltage  $V_{DD}$ . By setting the control pulse  $\phi_S$  to the H level and the dark output is accumulated in the accumulating capacitor 10. Subsequently, the control pulse  $\phi_{TX0}$  is set to the H level and the photo charges accumulated in the pn photodiode 24 are transferred to the accumulating capacitor 11 through the source-follower MOS transistor 5 and selection switch MOS transistor 6. The noise component is cancelled by the differential output amplifier 14 and the image signal  $V_{OUT}$  is generated. By supplying control pulses corresponding to the timing in Fig. 4, the charges can be added to two pn photodiodes 24 and the added charges can be read out.

By adding the switch MOS transistor, an image output having a high efficiency in the interlace scan can be

obtained in a manner similar to the second and third embodiments.

Fig. 10 shows a pixel cross sectional view of the fifth embodiment according to the invention. In the diagram, reference numeral 26 denotes a surface p+-type layer. The fifth embodiment is characterized in that the surface p+-type layer 26 constructs the photoelectric converting unit together with the n-type layer 25 and a pixel is formed by a buried type photodiode. With such a structure, a dark current which is generated in the surface can be suppressed. As compared with Fig. 9, since high photo charges of a good efficiency can be obtained, an image signal of a high S/N ratio and a high quality can be obtained.

According to the pixel of the structure shown in Fig. 10, a similar image output can be obtained by a timing of each control pulse which is provided in place of the pn photodiode 24 in Fig. 8 and is similar to that in the fourth embodiment.

According to the invention as described above, since a CMOS transistor type sensor in which the number of devices is reduced and a high numerical aperture and a fine structure can be obtained can be realized, there are advantages such as high yield due to an increase in integration, low costs, miniaturization of a package, and miniaturization of the optical system.

Since the addition and non-addition of the pixel signals can be realized by only a driving method, there is also an advantage such that the invention can cope with various operating methods including the conventional XY addressing function.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

#### Claims

1. A solid state image pickup apparatus for transferring charges generated by a photoelectric converting device to a floating diffusion portion through a transfer switch and for outputting a change in electric potential of said floating diffusion portion to an outside by a buffer amplifier, wherein  
a plurality of said photoelectric converting devices are connected to said one floating diffusion portion through a transfer switch and one set of said buffer amplifier is formed for a few pixels.
2. An apparatus according to claim 1, wherein said photoelectric converting device comprises an MOS transistor gate and a depletion layer under said gate.
3. An apparatus according to claim 2, wherein said

MOS transistor gate of said photoelectric converting device is formed by a same processing step as that of an MOS transistor of a peripheral circuit.

4. An apparatus according to claim 1, wherein said photoelectric converting device is a pn junction photodiode. 5
5. An apparatus according to claim 1, wherein the charges of a plurality of said photoelectric converting devices can be simultaneously or separately transferred to said floating diffusion portion. 10
6. An apparatus according to claim 1, wherein image signal outputs are obtained by arranging a plurality of solid state image pickup apparatuses. 15
7. An apparatus according to claim 6, wherein charges of at least two said photoelectric converting devices are added to said floating diffusion portion. 20
8. An apparatus according to claim 6, wherein upon reading of said photoelectric converting device, an image signal from a complementary color mosaic pattern is obtained synchronously with ODD and EVEN fields by an interlace scan. 25

30

35

40

45

50

55

FIG. 1

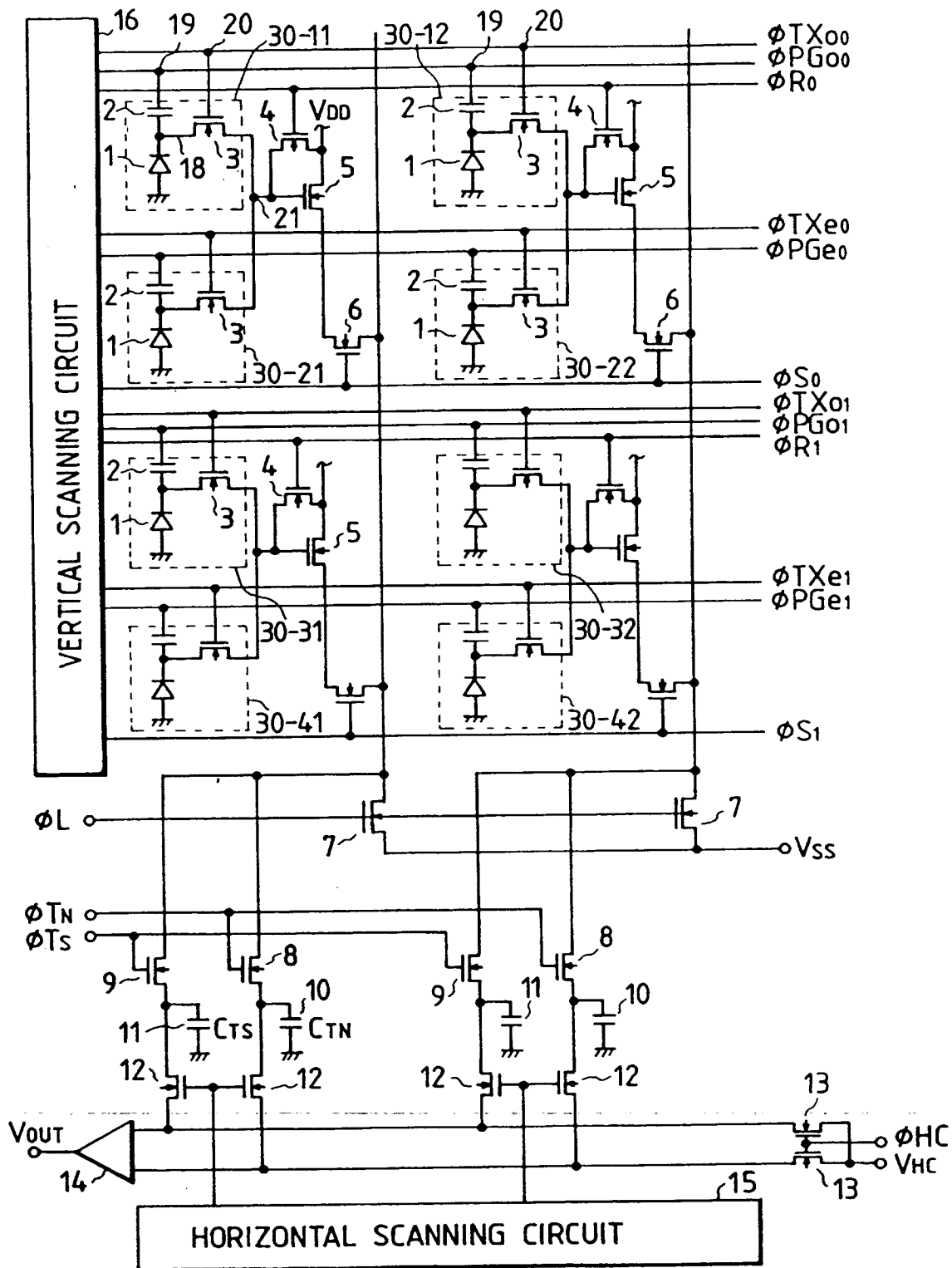




FIG. 2

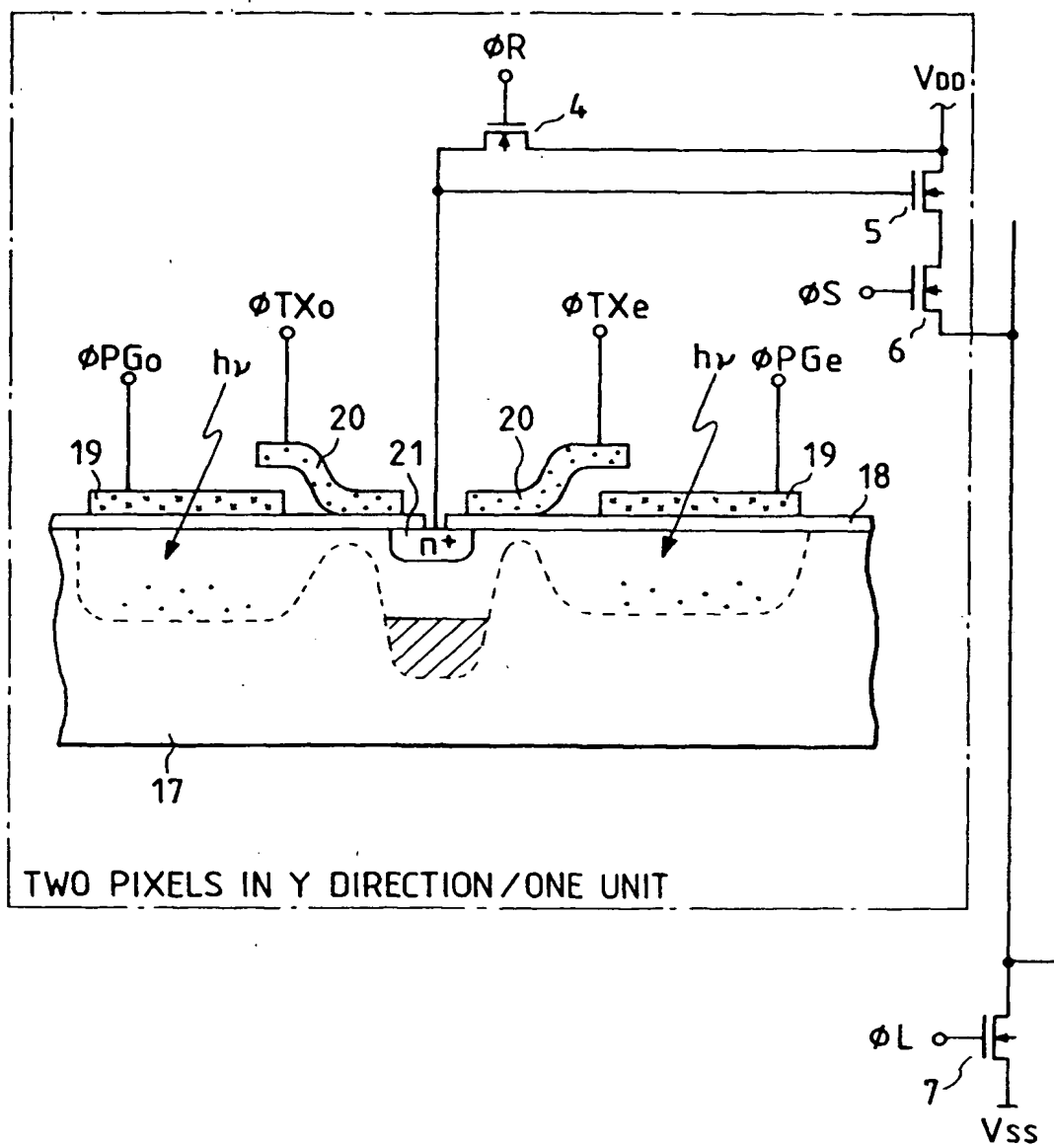


FIG. 3

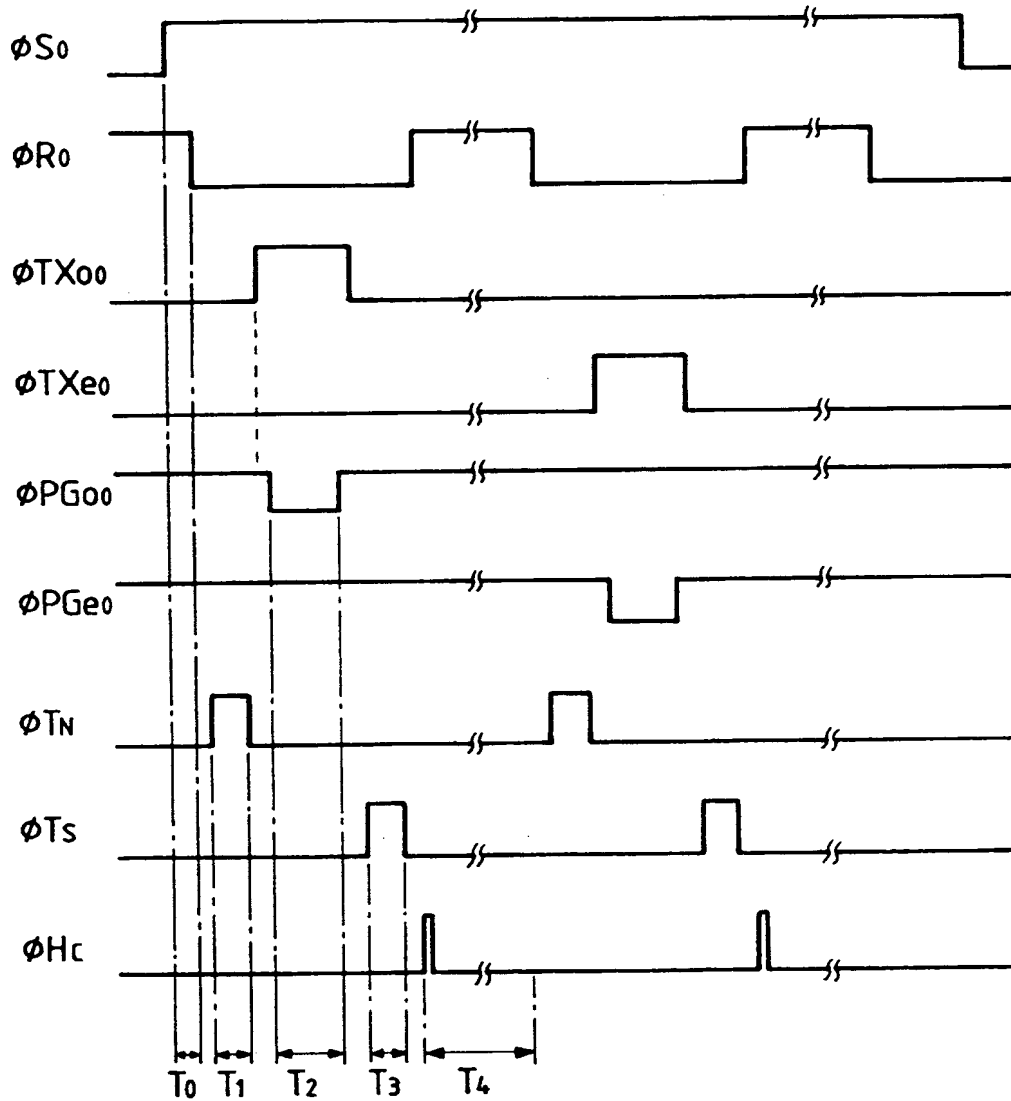


FIG. 4

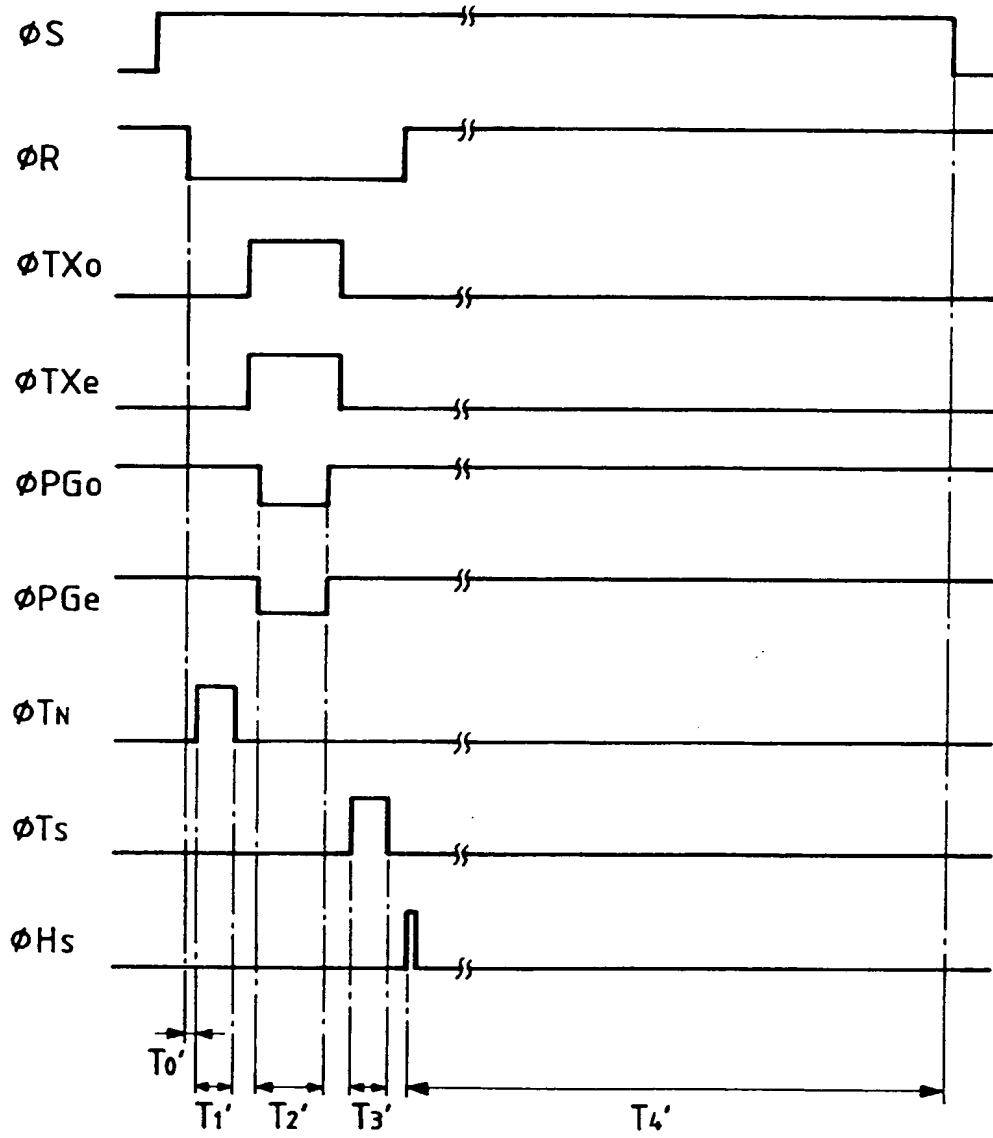
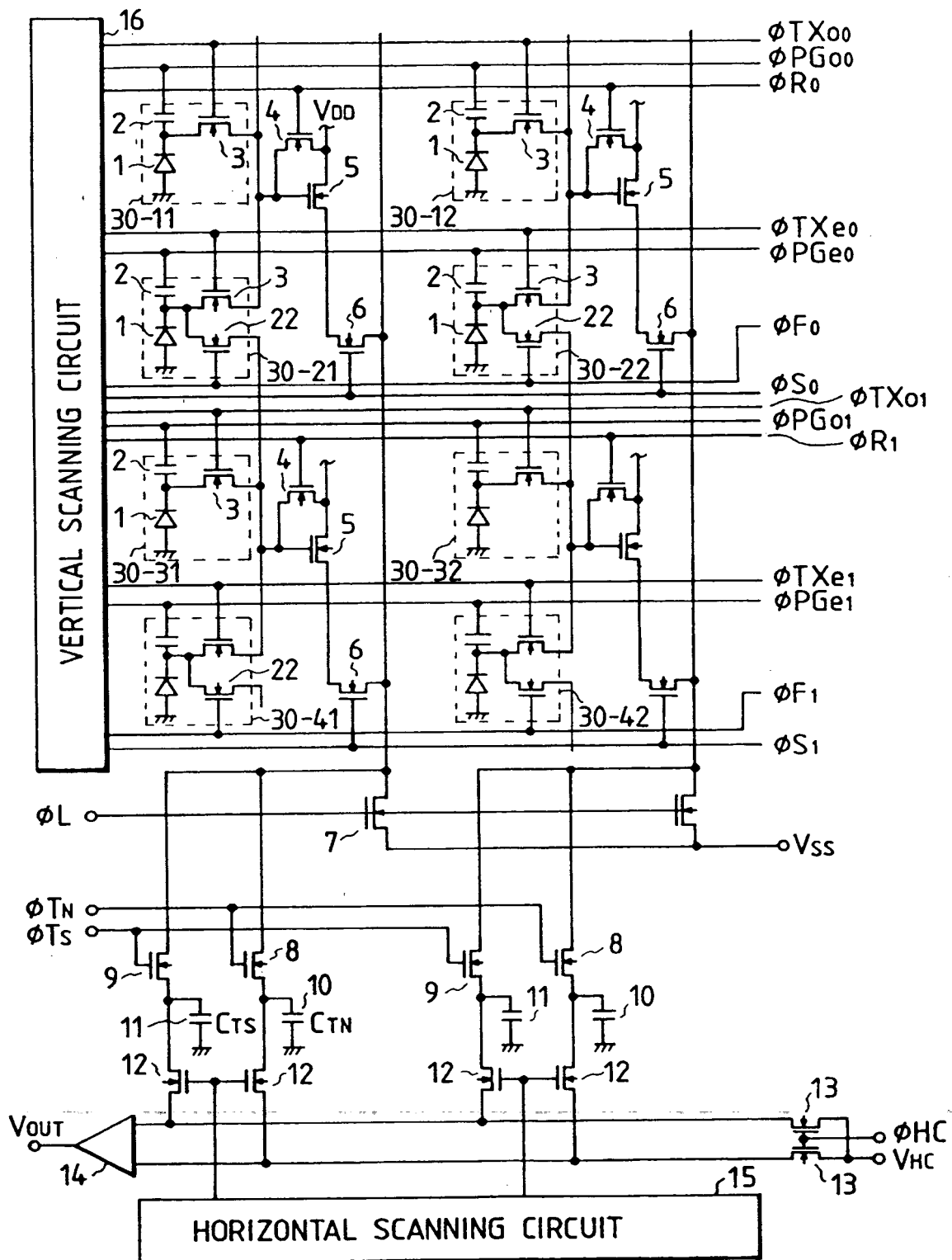


FIG. 5



*FIG. 6*

Cy	Ye
Mg	G
Cy	Ye
G	Mg

FIG. 7

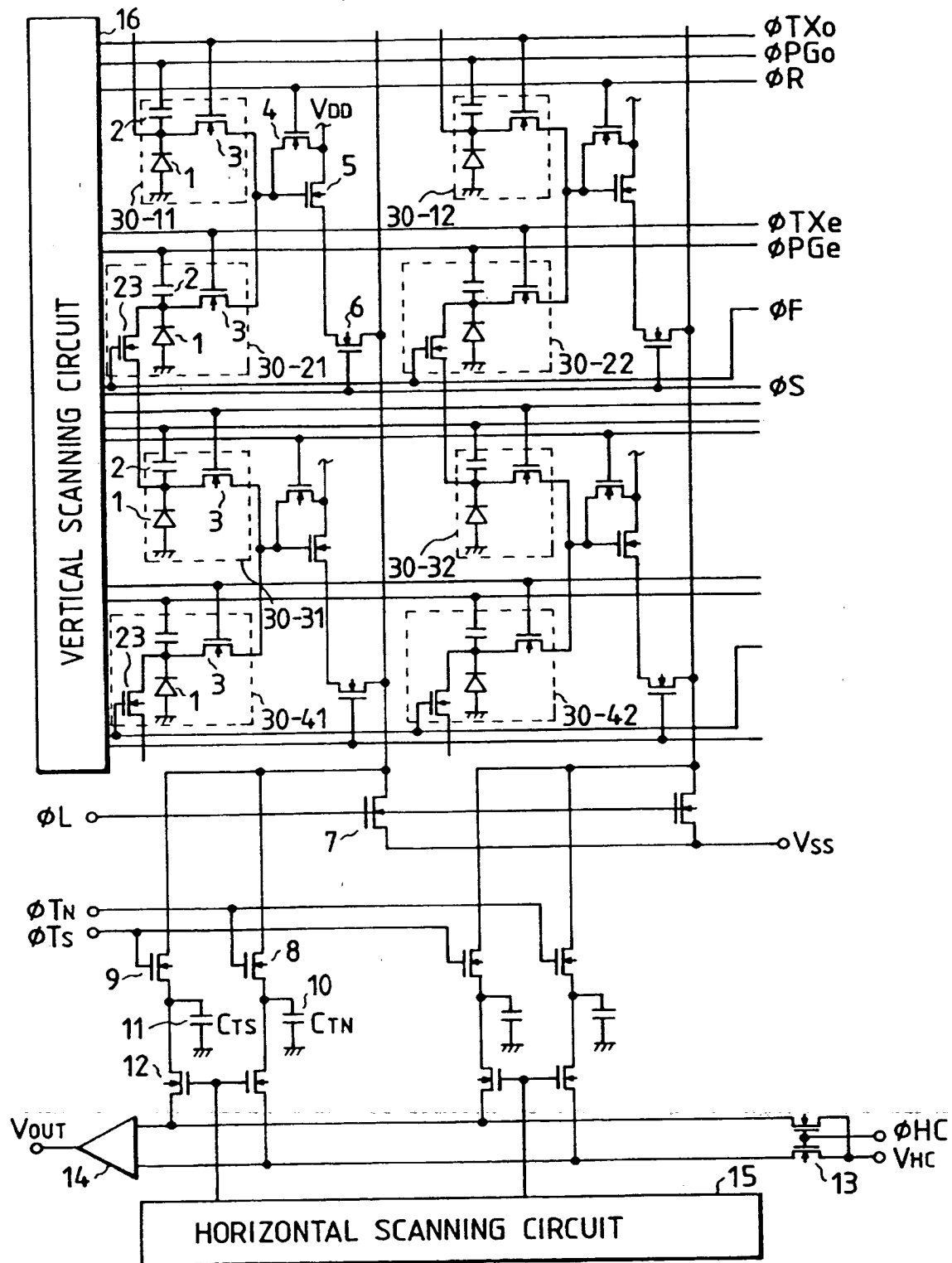


FIG. 8

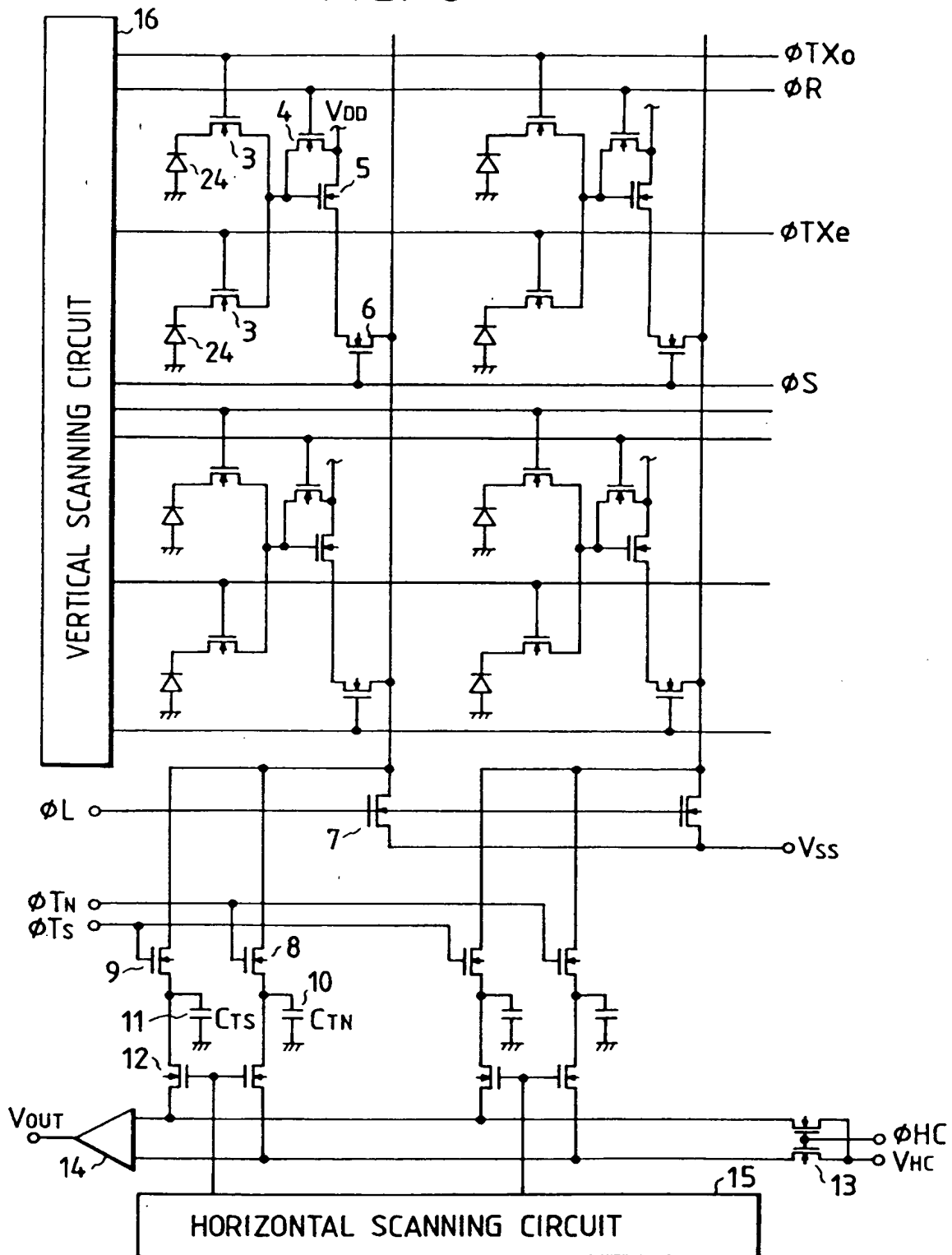


FIG. 9

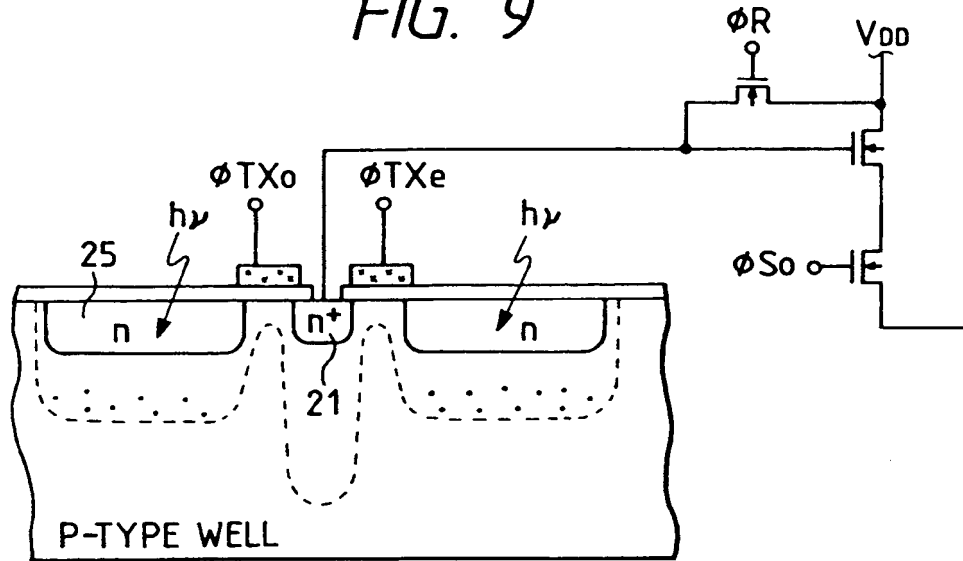


FIG. 10

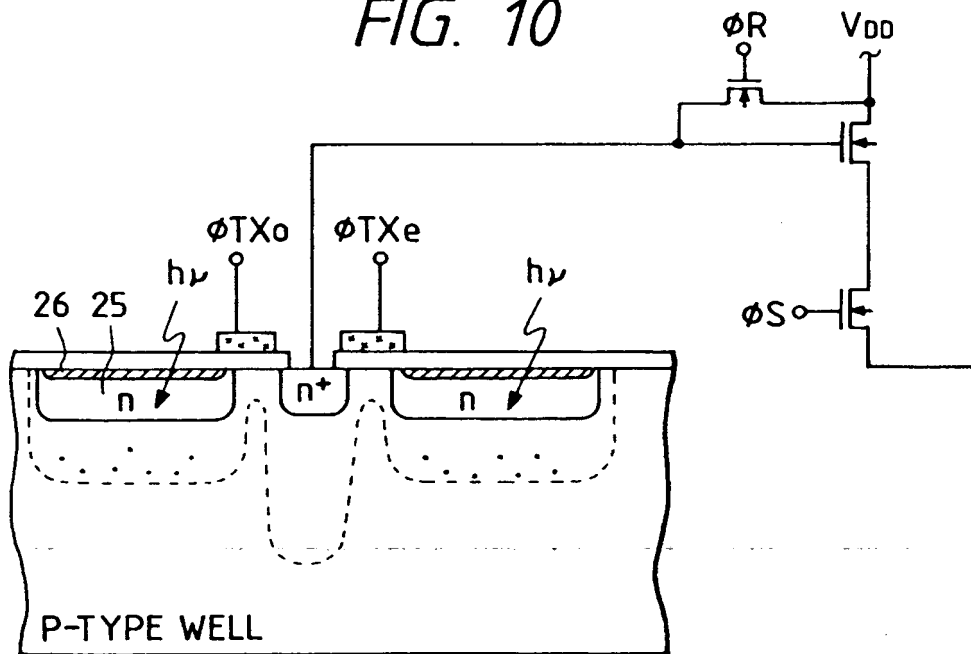
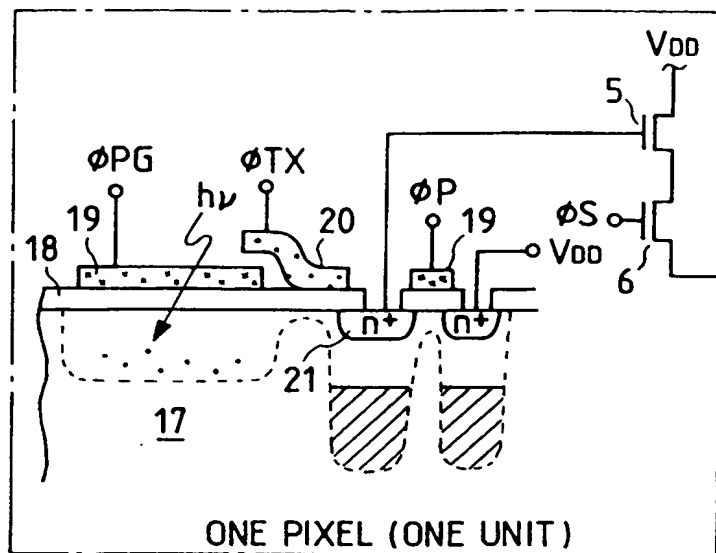




FIG. 11A



*FIG. 11B*

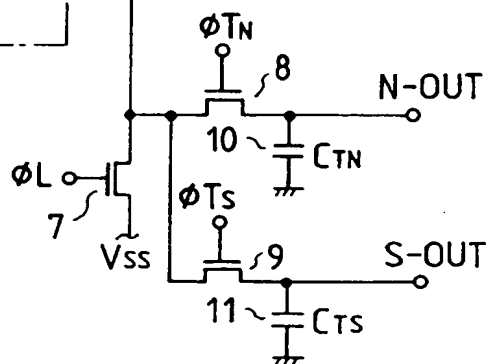
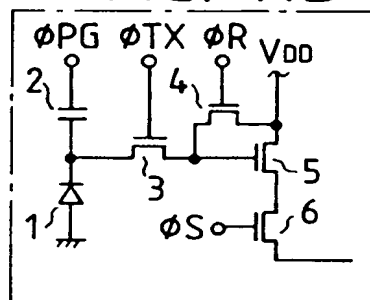


FIG. 11C

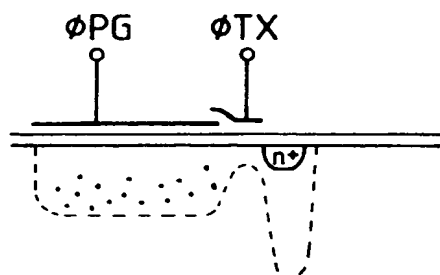
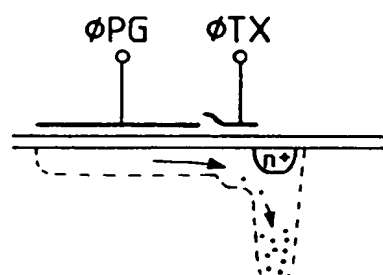


FIG. 11D



**THIS PAGE BLANK (USPTO)**



(12)

**EUROPEAN PATENT APPLICATION**

(88) Date of publication A3:  
22.04.1998 Bulletin 1998/17

(51) Int Cl.<sup>6</sup>: **H04N 9/07**, H04N 9/09,  
H04N 5/228, H04N 3/15

(43) Date of publication A2:  
05.02.1997 Bulletin 1997/06

(21) Application number: 96305660.1

(22) Date of filing: 31.07.1996

(84) Designated Contracting States:  
**DE ES FR GB IT NL**

(72) Inventor: **Takahashi, Hidekazu**  
**Tokyo (JP)**

(30) Priority: 02.08.1995 JP 197471/95

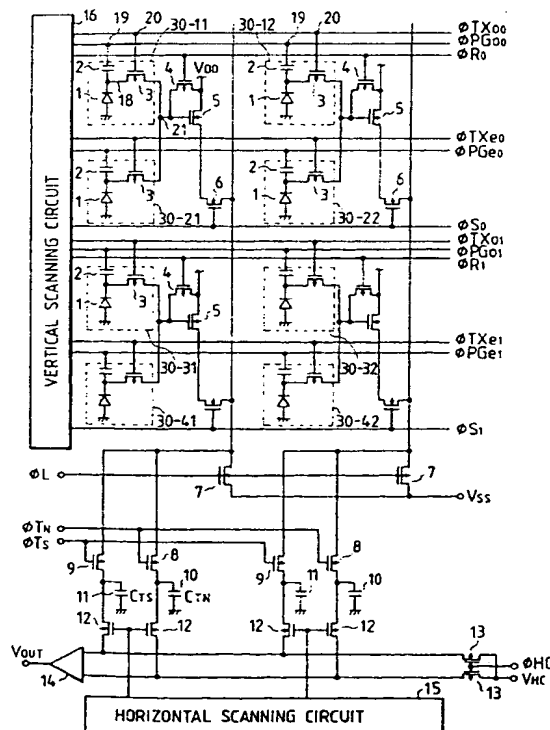
(74) Representative:  
Beresford, Keith Denis Lewis et al  
BERESFORD & Co.  
2-5 Warwick Court  
High Holborn  
London WC1R 5DJ (GB)

(71) Applicant: **CANON KABUSHIKI KAISHA**  
**Tokyo (JP)**

(54) **Solid state image pickup apparatus**

(57) In order to realize a multi-function sensor in which in a pixel portion an addition and a non-addition can be arbitrarily performed, there is provided a solid state image pickup apparatus in which charges generated by a photoelectric converting device are transferred to a floating diffusion portion through a transfer switch and a change in electric potential of the floating diffusion portion is outputted by a source-follower. Some photoelectric converting devices are connected to one floating diffusion portion through the transfer switch. One set of source-follower are formed for a few pixels. The photoelectric converting device is constructed by a MOS transistor gate and a depletion layer under the gate.

FIG 1





European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 96 30 5660

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 220 170 A (COX JOHN D ET AL) * column 3, line 52 - column 4, line 2: figure 3 *	1-7	H04N9/07 H04N9/09 H04N5/228 H04N3/15
X A	EP 0 481 373 A (SONY CORP) * page 3, column 2, line 30 - column 4, line 52: figure 1 *	1-4,6 5,7	
X	EP 0 576 104 A (CANON KK) * page 3, column 2, line 48 - page 4, column 3, line 48 * * page 6, column 7, line 15 - page 7, column 10, line 9; figures 3,4 * * page 10, column 15, line 33 - line 46: figure 9 *	1-4,6	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H04N
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>26 February 1998</b>	Examiner <b>De Paepe, W</b>
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons A : technological background O : non-written disclosure P : intermediate document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons A : technological background O : non-written disclosure P : intermediate document	

EP 0 757 476 A3 (1998-02-19)